WHAT IS CLAIMED IS:

1. An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to said SRAM array during a sleep mode

2. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} relative to a well voltage.

3. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array low supply voltage V_{ASS} relative to a substrate voltage.

4. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides a well voltage at about said high operating voltage V_{DD} during said sleep mode.

5. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on transistor parameters.

6. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller adjusts said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a process corner.

7. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller employs a component selected from the group consisting of:

a fuse,

a transistor,

a diode,

a ROM, and

a low-drop out regulator.

8. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller further provides a well voltage and said array high supply voltage V_{ADD}, said array low supply voltage V_{ASS} and said well voltage are provided as a set of optimum values for a general technology class of transistors.

9. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller adjusts said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a sleep mode current.

10. The SRAM device as recited in Claim 9 wherein said sleep mode voltage controller refines said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a diode leakage current.

11. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller further provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

12. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a minimum cell voltage for data retention.

13. The SRAM device as recited in Claim 1 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a minimum cell voltage for data retention and minimizing a total leakage current.

14. A method of operating an SRAM device, comprising:

employing in an integrated circuit an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

providing both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to said SRAM array during a sleep mode.

15. The method as recited in Claim 14 wherein said providing said array high supply voltage V_{ADD} is relative to a well voltage.

16. The method as recited in Claim 14 further comprising providing a well voltage at about said high operating voltage V_{DD} during said sleep mode.

17. The method as recited in Claim 14 wherein said providing said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} is based on transistor parameters.

18. The method as recited in Claim 14 further comprising adjusting said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a process corner.

19. The method as recited in Claim 14 wherein said providing employs a component selected from the group consisting of:

a fuse,

a transistor,

a diode,

a ROM, and

a low-drop out regulator.

20. The method as recited in Claim 14 further comprising providing a well voltage wherein said array high supply voltage V_{ADD}, said array low supply voltage V_{ASS} and said well voltage are provided as a set of optimum values for a general technology class of transistors.

21. The method as recited in Claim 14 further comprising adjusting said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a sleep mode current.

22. The method as recited in Claim 21 further comprising refining said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} based on a diode leakage current.

23. The method as recited in Claim 14 further comprising providing a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage and a voltage across a SRAM cell are all about a same voltage.

24. An SRAM device, comprising:

an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} and an array low supply voltage V_{ASS} to said SRAM array during a sleep mode and modify said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} during transition from an active mode to said sleep mode.

25. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller performs said modify based on reducing current leakage of said SRAM array and providing sufficient voltage across said SRAM array via said array high supply voltage V_{ADD} and said array low supply voltage V_{ASS} to retain data.

26. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller provides said array high supply voltage V_{ADD} lower than $V_{n\text{-}well}$ during said sleep mode.

27. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller provides said array low supply voltage V_{ASS} higher than a substrate voltage during said sleep mode.

28. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller is configured to regulate said array high supply voltage V_{ADD} relative to said array low supply voltage V_{ASS} during said sleep mode.

29. The SRAM device as recited in Claim 24 wherein said sleep mode voltage controller is configured to regulate said array low supply voltage V_{ASS} relative to said array high supply voltage V_{ADD} during said sleep mode.